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[Translation of the Annex to the International Preliminary Examination Report]

CLAIMS

Sub A2

1. A card (30) with a microprocessor (10) and contacts (22), the microprocessor (10) communicating with a terminal (20) by means of a communication device (40) in the form of a hard-wired circuit disposed between the contacts (22) and the microprocessor (10) and operating according to an asynchronous communication protocol with checking of the integrity of the signals transmitted, characterised in that said communication device (40) comprises means to return at least one information to the terminal (20) as a function of the signals received.

2. A card with a microprocessor and contacts according to Claim 1, characterised in that the communication device (40) comprises:

- a circuit (34) for analysing the electrical signals transmitted by the terminal (20) so as to supply a series of electrical pulses,
- a circuit (36) for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code (50) indicating the result of the check,
- a circuit (38) for determining each character from the pulses in the series,
- a first plurality of registers (42) for recording the characters of the command and the address supplied by the character determination

circuit (38) and making them available to the microprocessor (10),

- a second plurality of registers (44) for recording the characters of the data supplied by the character determination circuit (38) and making them available to the microprocessor (10),

- a circuit for acknowledging the command (52), associated with the first plurality of registers (42), for analysing the characters of the command and supplying a code (54) indicating the command reception status,

- a third plurality of registers (46) for recording the codes for the data and for the status of execution of the command supplied by the microprocessor (10), and

- a circuit (48) for transmitting to the terminal (20) the codes supplied by the checking circuit (36), the command acknowledgement circuit (52) and the third plurality of registers (46).

3. A card with a microprocessor and contacts according to Claim 2, characterised in that the analysis circuit (34) comprises means to detect the signals transmitted and to present them in the form of a series of electrical pulses of the binary type.

4. A card with a microprocessor and contacts according to Claim 2 or 3, characterised in that the checking circuit (36) comprises means to check the presence or not of a binary parity digit or a cyclic redundancy code and to supply a corresponding signal or code.

Add A3

Add C2